REMARKS

Claims 11-19 are the claims currently pending in the Application.

Objections to the Specification

Several paragraphs of the Specification are objected to because of informalities, including minor grammatical errors. These paragraphs are amended and therefore these objections should now be withdrawn.

Objection to Claims 12, 15 and 16

Claims 12, 15 and 16 are objected to because of informalities, including minor grammatical errors. These claims are amended and therefore these objections should now be withdrawn.

Rejection of Claims 11-19 under 35 U.S.C. § 112, First Paragraph

Claims 11-19 are rejected under 35 U.S.C. § 112, first paragraph, on the ground that the Specification does not describe subject matter presented in the claims (failure to satisfy the "written description" statutory requirement), as follows:

(a) independent claim 11 is rejected on the basis that the isolation of hardware and software as presented in the claim is not understood;

(b) independent claim 11 is rejected on the basis that isolating elements of the source code representing hardware units and software units is new matter not found in the original Specification;

(c) independent claim 11 is rejected on the grounds that modifying at least one element

of the source code elements based on a result of implementation of the evaluation function is new matter not found in original Specification;

(d) claim 12 is rejected on the ground that restructuring the source code based on the evaluated data transfer is not properly described in the Specification;

(e) claim 14 is rejected on the ground that feeding back a result of the performance evaluation of the bus to the step of structuring the source code to improve the architecture design is not properly described in the Specification;

(f) claim 14 is rejected on grounds similar to rejection 3(b);

(g) claim 15 is rejected on grounds similar to rejection 3(b);

(h) claim 16 is rejected on the ground that structuring the source code into elements representing hardware units and software units for use in the architecture design is not properly described in the Specification;

(i) claim 16 is rejected on grounds similar to rejection 3(b).

Further, claim 15 is rejected under 35 U.S.C. § 112, first paragraph, ("written description") on the ground that the Specification does not describe the optimization of the isolation of the source code into hardware and software elements; and,

claim 17 is rejected under 35 U.S.C. § 112, first paragraph, ("written description") on the ground that it is not understood why the number of times effecting data transfer on the bus is multiplied by n/m and is then divided by the processing rate and how this affects bus traffic or the processing rate evaluation and the design of the bus architecture.

These rejections are traversed.

In LSI (Large-Scale Integration) design and development process it is important to optimize hardware units and software units that are to be used. According to an

aspect of the present Application, hardware and software components that will be used in the design are both simulated using software written in general-purpose high-level programming language, such as the C or C++ programming languages or the like. (For example, see Specification, page 4, lines 1-5.) That is, a simulation program is written that includes software units to simulate the hardware components and further software units to simulate the software components.

With respect to the term "structuring of simulation platform" (or program) involving isolation of hardware and software described in the specification, Applicant notes as follows: The simulation platform or program is actually realized by the software; that is, the simulation platform described in the present invention provides the simulation environment in the algorithm design stage and is actually realized by the software described in the high-level general language. In LSI design, software for representing hardware elements and software elements is well known, wherein in the algorithm design stage, the hardware elements are expressed using the high-level programming language (e.g., C and C++ languages), whereas after the isolation between the hardware and software, they are expressed by RTL (register-transistor logic). In other words, the terms "hardware" and "software" used in the specification do not actually describe directly hardware elements and software elements, respectively.

The performance of this simulation program is then evaluated using a valuation function that counts traffic using a software unit of the simulation program called a "bus" that interconnects the software modules that model hardware components with the software modules that model software. (For example, see Specification, page 4, lines 5-13.) According to an aspect of Applicant's invention, this software unit called the bus is used for counting traffic to evaluate the overall design. (For example, see Specification, page 4, lines 5-13.)

According to a further aspect of Applicant's disclosure, a result of the evaluation process based on the bus performance, as discussed, is fed back to the structuring process, such that the isolation of the "hardware" components and the "software" components is optimized in response to the bus traffic, in order to optimize the overall design (for example, see Specification, page 4, lines 5-13; page 5, lines 1-5).

Therefore, the isolation of the software and the hardware features in the claims, and the evaluation process using the bus features, are fully supported by the original Specification. Further, the claims will be readily understood by a person of ordinary skill in the art in the light of Applicant's original Disclosure. Accordingly, the 35 U.S.C. § 112, first paragraph, rejections should now be withdrawn.

Rejection of Claims 11-15 and 18 under 35 U.S.C. § 103

Claims 11-15 and 18 are rejected under 35 U.S.C. § 103 as being obvious from Chang et al., U.S. Patent No. 6,269,467 and Tseng et al., U.S. Patent No. 6,321,366 and Swoboda et al., U.S. Patent No. 6,546,505 in view of Fujiwara et al, U.S., Patent No. 6,510,541. This rejection is traversed.

The cited references do not disclose or suggest the above-cited features of Applicant's claim invention. By way of example, independent claim 11 requires isolating elements of the source code representing hardware units and software units.

Chang discloses a block design methodology for design of circuits, in which the experience of the designer regarding the pre-design circuit blocks is taken into account in forming block specifications for circuit blocks on the floor plan collection (Chang, Abstract). Chang discloses bus verification for multi-block designs (Chang, column 5, lines 8-19). Chang

refers to the chip level and floor plan; hence, this patent teaches the implementation in which the RTL description put into the LSI. In short, this patent merely describes a method for putting the algorithm design into RTL description; in other words this patent is directed to the after-processing, which is irrelevant to the present invention.

Chang does not disclose or suggest isolating elements of the source code representing hardware units and software units, as *inter alia*, required by independent claim 11. Since Chang does not disclose or suggest this feature, Chang is incapable of disclosing or suggesting modifying source code elements based on a result of implementation of the evaluation function, the evaluation function evaluating data transfer that occurs on the bus, as further required by independent claim 11.

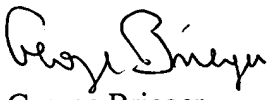
The remaining references, do not cure the deficiencies of Chang as they relate to Applicant's invention as claimed in independent claim 11. Tseng is related to a TIFG logic device, whereas the present invention teaches isolation of hardware and software. Swoboda teaches semiconductor chips and is related to LSI testing, and discloses methods to compile, assemble, and link software code (described in high-level programming languages, performed in the prescribed stage of LSI testing). That is, Swoboda teaches how to put algorithm design into the RTL description, which merely corresponds to the after-processing, unlike with the present invention. Fujiwara is directed to chips and LSI, and discloses an implementation for putting the RTL description into the LSI. Therefore, Chang and the other cited references, even if taken together in combination as a whole, do not disclose or suggest the recitations of independent claim 11.

Claims 12-19 depend from independent claim 11 and thus incorporate novel and nonobvious recitations thereof. Accordingly, claims 12-19 are patentably distinguishable over

the prior art for at least the reasons that independent claim 11 is patentably distinguishable over the prior art. Therefore, this rejection should now be withdrawn.

For at least the reasons set forth in the foregoing discussion, Applicant believes that the Application is now allowable, and respectfully requests that the Examiner reconsider the rejections and allow the Application. Should the Examiner have any questions regarding this Amendment, or regarding the Application generally, the Examiner is invited to telephone the undersigned attorney.

Respectfully submitted,



George Brieger
Registration No.: 52,652

Scully, Scott, Murphy & Presser
400 Garden City Plaza
Suite 300
Garden City, New York 11530
(516) 742-4343 Ext . 503
GB:ae